REMARKS

The specification has been amended to secure correspondence with the drawings.

Claims 36, 39 and 42 have been amended. Support for the amendment of Claims 36, 39 and 42 appears in the specification at least at: page 14, lines 18-32; page 21, lines 4-12 and in FIGS. 1-5, 7E-7F.

Claims 36-38 are novel over Kinsman (6,172,419).

Regarding Kinsman, the Examiner states:

> Kinsman discloses a semiconductor package device (36) a **substrate having a first surface (102)** ... and central through hole between the first and second surfaces (see Figure 2); ... **a semiconductor chip (120)** in said through hole, **wherein the semiconductor chip (120) has a first surface flush with the first surface of the substrate (102)** ... (Office Action, pages 2-3, emphasis added.)

However, Kinsman teaches that the "first surface" of "the semiconductor chip (120)" is mounted to a thin sheet material 116. Thus, the Examiner has failed to callout where Kinsman teaches or suggests that the "first surface" of "the semiconductor chip (120)" is exposed.

Specifically, Kinsman teaches:

> An upward facing cavity is formed by securing a support base such as thin sheet material 116 to the bottom of substrate 102 to cover aperture 114. ... The dimensions (length and width) of the thin sheet material 116 are greater than the dimensions (length and width) of aperture 114 so as to completely cover aperture 114, but typically less than the dimensions (length and width) of substrate 102. BGA package 100 further comprises a **semiconductor element or die 120 mounted in the cavity formed by the aperture 114 and thin sheet material 116**, which minimizes the effect of die thickness on the overall package height. (Col. 4, line 50 to Col. 5, line 2, emphasis added.)

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For at least the above reasons, Kinsman does not teach or suggest:

> A stackable semiconductor package comprising:
> a substrate having a first surface, an opposite second surface, and central through hole between the first and second surfaces;
> a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces include a plurality of lands, the circuit patterns of the second surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;
> a semiconductor chip in the through hole, **wherein the semiconductor chip has a first surface flush with the first surface of the substrate**, and an opposite second surface including a plurality of conductive pads, the pads being oriented in a same direction as the second surface of the substrate, **wherein the first surface of the semiconductor chip is exposed**;
> a plurality of conductive connecting means, wherein each of the conductive connecting means is electrically connected between a respective one of the pads of the second surface of the semiconductor chip and a respective one of the bond fingers of the circuit patterns of the second surface of the substrate;
> a hardened encapsulant within the through hole and covering the semiconductor chip therein, the bond fingers, the pads, and the conductive connecting means, wherein the lands of the circuit patterns of each of the first and second surfaces of the substrate are outward of a perimeter of the encapsulant; and
> a plurality of electrically conductive balls each fused to a respective one of the lands of the circuit patterns of the first surface of the substrate,

as recited in amended Claim 36, emphasis added.

As set forth in Applicants specification at page 14, lines 29-32:

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> In addition, **the first major surface 30a of the semiconductor chip 30 is exposed without being covered** with the resin encapsulate 50, **so that it can easily discharge heat generated therefrom.** (As amended, emphasis added.)

For at least the above reason, Claim 36 is allowable over Kinsman. Claims 37-38, which depend from Claim 36, are allowable for at least the same reasons as Claim 36.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 39-42 are allowable over Kinsman in view of Akram et al. (6,313,522).

Claim 39 is allowable over Kinsman for reasons similar to those discussed above regarding Claim 36. Akram et al. does not cure the deficiency in Kinsman.

Specifically, in reference to FIG. 5, Akram et al. teaches:

> In the illustrated embodiment of FIG. 5, **the interconnect devices 51, 52, 53 function to provide a structural interface for the semiconductor devices 20, 22, 24, respectively.** The interconnect devices 51, 52, 53 may comprise a flex circuit without any conductive wires, and thus, is non-conductive, or a flex circuit in which there is no electrical connection with the conductive wires. **The interconnect devices 51, 52, 53 are coupled to the substrates 14, 16, 18, respectively, using an appropriate adhesive 60 or other suitable fastening means.**
>
> **The semiconductor devices 14, 16, 18 are mounted on the interconnect devices 51, 52, 53, respectively, using an appropriate adhesive 62** or other suitable semiconductor fastening means, such that the semiconductor devices 14, 16, 18 are positioned within respective openings 14D, 16D, 18D of the respective substrates 14, 16, 18. (Col. 12, line 7 to line 22, emphasis added.)

Accordingly, Akram et al. teaches that the lower surfaces of the semiconductor devices 20, 22, 24 are mounted on the interconnect devices 51, 52, 53, respectively. Thus, Kinsman

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and Akram et al., either alone or in combination, do not teach or suggest:

A stack of semiconductor packages comprising:

a first semiconductor package and a second semiconductor package;

the first semiconductor package comprising: a substrate having a first surface, an opposite second surface, and central through hole between the first and second surfaces; a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces include a plurality of lands, the circuit patterns of the second surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface; a semiconductor chip in the through hole, **wherein the semiconductor chip has a first surface flush with the first surface of the substrate**, and an opposite second surface including a plurality of conductive pads, the pads being oriented in a same direction as the second surface of the substrate, **wherein the first surface of the semiconductor chip is exposed**; a plurality of conductive connecting means, wherein each of the conductive connecting means is electrically connected between a respective one of the pads of the second surface of the semiconductor chip and a respective one of the bond fingers of the circuit patterns of the second surface of the substrate; a hardened encapsulant within the through hole and covering the semiconductor chip therein, the bond fingers, the pads, and the conductive connecting means, wherein the lands of the circuit patterns of each of the first and second surfaces of the substrate are outward of a perimeter of the encapsulant; and a plurality of electrically conductive balls each fused to a respective one of the lands of the circuit patterns of the first surface of the substrate; and

the second semiconductor package comprising a second substrate including second circuit patterns, a second semiconductor chip electrically coupled to the second circuit patterns, and second conductive balls fused the second circuit patterns, wherein the second semiconductor chip is electrically coupled to the second conductive balls through the second circuit patterns,

wherein the second semiconductor package is in a stack with the first semiconductor package, and at least some of the second conductive balls of the second package each superimpose and are electrically connected

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to respective ones of the lands of the circuit patterns of the second surface of the substrate of the first semiconductor package,

as recited in amended Claim 39, emphasis added. Accordingly, Claim 39 is allowable over Kinsman in view of Akram et al. Claim 40, which depends from Claim 39, is allowable for at least the same reasons as Claim 39.

Claims 42 is allowable for reasons similar to Claim 39. Claim 41, which depends from Claim 42, is allowable for at least the same reasons as Claim 42.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 36-42 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 3, 2005.

Attorney for Applicant(s) — June 3, 2005 Date of Signature

Respectfully submitted,

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